DETAILED ACTION

1. This action is responsive to communication filed 07/26/2010.

2. Claims 1-14 are pending for examination. Claims 1 and 8 are independent claims. Claims 15-16 had been cancelled.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/26/2010 has been entered.

Claim Rejections - 35 USC § 112

5he following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 4-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following term lack antecedent basis:

i. The at least one of a plurality of CPU's – claim 4.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brenner et al. (US 6,658,449 B1).

7. Brenner et al. was submitted in IDS filed on 6/24/2005.

8. As per claim 1, Brenner teaches the invention substantially as claimed including a method comprising:

receiving a transaction request (fig. 8, element 810; col. 3, lines 26-27);

selecting at least one central processing unit in a computing system, the computing system comprising at least one central processing unit (fig. 8, elements 860 & 870);

polling the selected at least one central processing unit to determine the current load on the selected at least one central processing unit (fig. 8, element 870; fig. 9, element 910; fig. 10, element 1020; wherein the current load of the at least selected one central processing unit is zero, in other word, the CPU is idle and it has no load);

identifying any of the selected at least one central processing unit whose current load is idle and allocating the transaction request to at least one of the identified at least one central processing unit (col. 2, lines 5-7; col. 4, lines 44-50); and,

if the current load for all of the selected at least one central processing unit is not idle (the CPU has load) , delaying execution of the transaction request for a predetermined time delay, or until polling determines that the current load is idle for at least one of the selected central processing units (col. 2, lines 5-8; col. 5, lines 11-13; col. 10, line 6-17, wherein if there is no idle processor available, the transaction is placed in a global queue until an idle processor is available which is delaying execution of the transaction until an idle processor is found);

wherein said polling, allocating, and delaying steps are performed on at least one particular machine, said at least one particular machine comprising at least one physical computing device (abs; col. 9, lines 32-44).

9. Brenner does not explicitly teach a threshold wherein the current load is below a threshold and wherein the current load is above a threshold. However, Brenner teaches determining whether there is at least one idle processor (has no load), in other words, the processor current load is below the threshold of having at least one job which is the current load is below a threshold as claimed. Brenner teaches if all the processors' current load is equal or above one job (not available= not idle), which is all processor current load above a threshold as claimed.

10. As per claim 2, Brenner teaches polling at defined time intervals to determine the system load (abs.; col. 1, lines 53-64).

11. As per claim 3, Brenner teaches polling continues until the current load drops below the predetermined threshold, at which time the transaction request is allocated (col. 1, lines 53-64; col.5, lines 10-15; col.5, lines 32-37; col. 10, lines 6-17).

12. As per claim 4, Brenner teaches the predetermined threshold is achieved when the at least one of a plurality of CPU's becomes idle (fig. 8, element 870; fig. 9, element 910; fig. 10, element 1020; col. 2, lines 5-11; col. 4, lines 44-50; col. 4, lines 57-65).

13. As per claim 8, Brenner teaches the invention substantially as claimed including a system comprising:

a computing system comprising at least one central processing unit (fig. 2, elements 230-280);

a scheduling computer for scheduling a transaction, the scheduling computer, on receipt of a transaction request (fig. 8, element 810; col. 3, lines 26-27), polling at least one central processing unit of the computing system to obtain a value for the current central processing unit load (fig. 8, element 870; fig. 9, element 910; fig. 10, element 1020; wherein the current load of the at least selected one central processing unit is zero, in other word, the CPU is idle and it has no load);

the scheduling computer, allocating the transaction request to one of the polled at least one central processing unit if the current load of the polled at least one central processing unit is idle, or delaying execution of the transaction request for a predetermined time period if the current load on the polled at least one central processing unit is not idle (col. 2, lines 5-8; col. 5,

lines 11-13; col. 10, line 6-17, wherein if there is no idle processor available, the transaction is placed in a global queue until an idle processor is available which is delaying execution of the transaction until an idle processor is found).

14. Brenner does not explicitly teach a predetermined threshold wherein the current load is below a predetermined threshold and wherein the current load is above the predetermined threshold and the predetermined threshold stored on a scheduling computer;. However, Brenner teaches determining whether there is at least one idle processor (has no load), in other words, the processor current load is below the threshold of having at least one job which is the current load is below a threshold as claimed. Brenner teaches if all the processors' current load is equal or above one job (not available= not idle), which is all processor current load above a threshold as claimed. Brenner does not explicitly teach that the threshold is stored on a scheduling computer. However, it is well known to one of ordinary skill in the art at the time the invention is made that in order for the system to search for idle processor, it must search for a value stored in the system to verify idleness. As evidence, claim 11, dependent of the instant claim discloses that the threshold is achieved by one of the CPUs becomes idle.

15. As per claim 9, Brenner teaches the scheduling computer continue to poll the computing system at defined time intervals to determine the current load of at least one central processing unit of the computing system (abs.; col. 1, lines 53-64; col. 7, lines 9-13; wherein periodic load balancing is polling at defined time interval to determine the current load of the CPUs).

16. As per claim 10, Brenner teaches the scheduling computer allocate the transaction when the scheduling computer determines that the current load has dropped below the predetermined threshold(col. 1, lines 53-64; col.5, lines 10-15; col.5, lines 32-37; col. 10, lines 6-17).

17. As per claim 11, Brenner teaches the predetermined threshold is achieved when the at least one of the computing system central processing units becomes idle(fig. 8, element 870; fig. 9, element 910; fig. 10, element 1020; col. 2, lines 5-11; col. 4, lines 44-50; col. 4, lines 57-65).

18. Claims 5-7 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brenner et al. (US 6,658,449 B1), in view of Robsman (S 6,477,561 B1).

19. As per claim 5, Brenner does not explicitly teach wherein the predetermined time delay does not exceed 1000 milliseconds.

20. However, Robsman teaches delaying execution of the transaction request for a predetermined time delay (abs.; col. 2, lines 4-6; col. 2, lines 18-24).

21. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Brenner of initial and periodic load balancing load balancing and Robsman teaching because one would be motivated to use Robsman teaching of limiting the active threads count by delaying thread execution based on CPU utilization to be implemented in Brenner system to limit the number of thread that can be dispatch to a CPU at a

time in order to manage the load across the system.

22. The combined teaching of Brenner and Robsman does not explicitly teach time delay does not exceed 1000 milliseconds.

23. However, it would be obvious to one of ordinary skill in the art at the time the invention was made that the delay time does not exceed 1000 milliseconds is set based on design choice.

24. As per claim 6, Brenner does not explicitly teach the predetermined time delay does not exceed 500 milliseconds.

25. However, Robsman teaches delaying execution of the transaction request for a predetermined time delay (abs.; col. 2, lines 4-6; col. 2, lines 18-24).

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Brenner of initial and periodic load balancing load balancing and Robsman teaching because one would be motivated to use Robsman teaching of limiting the active threads count by delaying thread execution based on CPU utilization to be implemented in Brenner system to limit the number of thread that can be dispatch to a CPU at a time in order to manage the load across the system.

27. The combined teaching of Brenner and Robsman does not explicitly teach the predetermined time delay does not exceed 500 milliseconds.

28. However, it would be obvious to one of ordinary skill in the art at the time the invention was made that the predetermined time delay does not exceed 500 milliseconds is set based on design choice.

29. As per claim 7, Brenner does not explicitly teach that the predetermined time delay is in the order of one to fifteen time slice intervals.

30. However, Robsman teaches delaying execution of the transaction request for a predetermined time delay (abs.; col. 2, lines 4-6; col. 2, lines 18-24).

31. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Brenner of initial and periodic load balancing load balancing and Robsman teaching because one would be motivated to use Robsman teaching of limiting the active threads count by delaying thread execution based on CPU utilization to be implemented in Brenner system to limit the number of thread that can be dispatch to a CPU at a time in order to manage the load across the system.

32. The combined teaching of Brenner and Robsman does not explicitly teach the predetermined time delay is in the order of one to fifteen time slice intervals.

33. However, it would be obvious to one of ordinary skill in the art at the time the invention was made that the predetermined time delay is in the order of one to fifteen time slice intervals is set based on design choice.

34. As per claims 12-14, they are the system claims of the method claims 5-7 respectively. Therefore, they are rejected under the same rational.

Remarks

33. Applicant is requested to provide support in the specification for the following:

    a. "a predetermined threshold stored on a scheduling computer", claim 8.

34. If applicant fails to provide proper support of the above limitations in the specification, applicant is suggested to amend the claims to comply with the specification; otherwise 112 first rejection will be raised in the next office action.

Response to Arguments

33. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE H. ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 8:00 AM to 2:00 PM.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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